Sid Rajpurohit

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RTL AND FPGA DESIGN | COMPUTER ARCHITECTURE | HARDWARE VALIDATION

EDUCATION

Rochester Institute of Technology
Bachelor of Science in Computer Engineering *Expected May 2027*
Current coursework: Design of Computer Systems (EEEE-521), Machine Intelligence
Selected coursework: Computer Architecture, Digital Systems Design I & II, Digital Signal Processing

TECHNICAL SKILLS

Languages: VHDL, Verilog, C, C++, Python, MATLAB, Tcl, Bash
Design and verification: Vivado, Quartus, ModelSim, RTL design, testbenches, FPGA debugging
Platforms and lab: Basys3, MAX10, Red Pitaya, PYNQ, AXI GPIO, Git, Linux, oscilloscopes, DMMs

EXPERIENCE

Systems Engineer Co-Op January 2026 – May 2026
SmartKable
- Role focused on LineRanger installation-data analysis and technical recommendations for electrical distribution systems.
- Responsibilities included Excel modeling, data analysis, and draft engineering reports with the Systems Engineer team.

Computer/Electrical Engineering Intern January 2025 – August 2025
MKS Inc. *Rochester, NY*
- Implemented VHDL direct digital synthesis (DDS) logic with a 32-bit phase accumulator, 14-bit samples, and amplitude control; integrated Red Pitaya FPGA controls through PYNQ and AXI.
- Built Python/Jupyter routines for ADC/DAC and GPIO control and NumPy FFT analysis; scripted Vivado workflows with Tcl and Bash.
- Performed prototype bench testing, GaN FET thermal testing, and precision soldering.

Lab Conductor August 2023 – Present
Rochester Institute of Technology *Rochester, NY*
- Teach VHDL, C, and FPGA debugging in Digital Systems Design I & II and Applied in C labs; diagnose logic and board-mapping issues and author instructional material.

PROJECTS AND RESEARCH

Pipelined MIPS Processor | *VHDL, Verilog, Basys3, ModelSim*
- Designed a five-stage MIPS datapath and control logic with pipeline registers, hazard detection, and forwarding to handle instruction dependencies.
- Verified arithmetic and load/store behavior through simulation and a Fibonacci test program; tested the processor prototype on Basys3 FPGA hardware.

14-bit RISC Processor | *Verilog, Quartus, ModelSim* In progress
- Extend the DCS processor RTL for arithmetic, logic, and register-transfer instructions; debug status flags in a Harvard architecture with separately mapped I/O.
- Exercise instruction behavior using ModelSim testbenches and memory initialization programs; trace waveforms to isolate datapath and control errors.

HDC Hardware Accelerator Research | *RIT* Ongoing
- Investigate hyperdimensional computing (HDC) with Dr. Sathwika Bavikadi, focusing on TorchHD classification workflows for ISOLET and MNIST.
- Study encoding, binding, bundling, and similarity search to identify operations shared across HDC workloads.
- Architecture goal: reusable compute units and memory organization balancing latency and hardware resource use.

Flightseeing Owl Drone | *Multidisciplinary Senior Design* In progress
- Compare camera, live-video, and GPS options against field-of-view, payload, and integration requirements; serve as client contact for the museum's drone project and coordinate design reviews.
- Planned integration scope: embedded software, flight-controller/GPS interfaces, telemetry, and system validation.